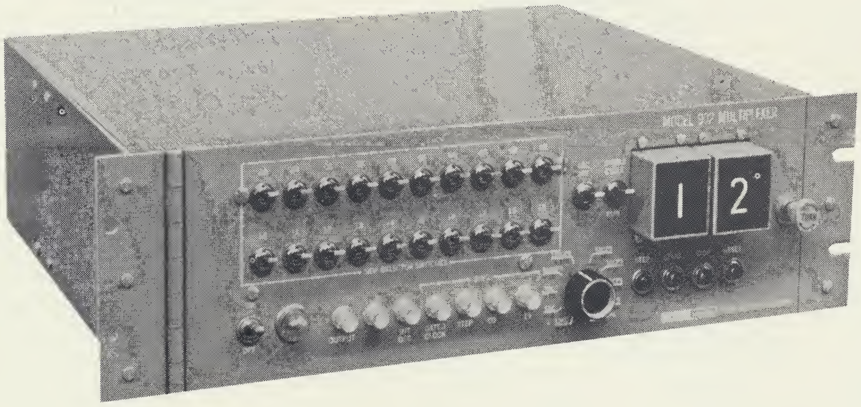
DATA SYSTEMS DIVISION

harman kardon

PLAINVIEW, N. Y. OVERBROOK 1-4000

MODEL 902
20 CHANNEL MULTIPLEXER



902 – SOLID STATE
– 20 CHANNEL
– HIGH SPEED
– MULTIPLEXER

For precise, high speed multiplexing of 20 channels (or more) of analog data, the Model 902 offers every convenience and useful feature. This unit utilizes the precision switching performance of the MX-260 Multiplex Switch to attain its phenomenal input-output isolation and accuracy, and couples this capability with:

- Bipolar Analog operation, ±15 volts
- Versatile frequency variability
- Internal or external synchronization
- Front-panel controlled channel skipping
- Externally controlled channel skipping
- Continuous or single-cycle operation
- Step, Frame, and Clock sync outputs
- Nixie channel number indicators

Performance includes operation, synchronously, or asynchronously, to 10Kc, with typical leakage current of .06 ua, offset of 100 uv, and series impedance of 36 ohms.

Additional Model 902 units may be stacked to provide unlimited channel expansion.

Designed from the start for systems use, the Model 902 uses H–K logic modules and Flexi-Cards* exclusively and will therefore meet rigorous environmental requirements.

Model 902: $3250

902 MULTIPLEXER

DSD — HK

SPECIFICATIONS

SIGNAL SPECIFICATIONS

Number of channels	20
Maximum Analog voltage	±15 volts*
Maximum load current	1 ma
Stepping rate	Variable 1 cps – 10Kc
Skip speed	4 μs per channel
Normal switching speed	20 μs
Effective series impedance	36 ohms max
Offset voltage	100 μv max
Leakage current	.06 μa max (25°C)**
Maximum noise	100 μv rms
Shunt capacitance	50 pf (unselected channel)
Shunt output capacitance	100 pf max

* *Maximum voltage between adjacent channels should not exceed 15 volts.*

** *This is maximum leakage current, worst conditions. The effect of this current must be added to offset voltage to determine offset error. This leakage current will be proportionately less, for low level input signals.*

INPUT POWER

115 vac, 60 cps, 1a.

FRONT PANEL CONTROLS

Frequency Selector Switch
Internal/External Clock Selector
Single Cycle/Continuous Selector
Manual Reset
Manual Stop
Manual Start
Manual Single Step
Channel Skip (20)
Power ON/OFF

ENVIRONMENTAL

Temperature, Operating	–30°C to +71°C
Temperature, Storage	–62°C to +85°C
Mounting	Any position

Designed to meet the general requirements of MIL-E-5272C

MECHANICAL

Size	5 1/4" x 19" x 14 1/2"
Color	Harman-Kardon Blue
Weight	22 lbs.
Internal Construction	Plug-in Harman-Kardon Flexi-Cards*
Mounting Dimensions	Standard RETMA

SYSTEMS CONNECTORS

J101
AMPHENOL 57–40240
(Mates With 57–30240)

PIN	FUNCTION	
1	External Start	Input
2	External Stop	Input
3	External Advance	Input
4	Step Sync	Output
5	External Reset	Input
6	Gated Clock Sync	Output
7	Internal Clock	Output
8	External Clock, 1 Volt	Input
9	Frame Sync (19)	Output
10	Frame Sync (00)	Output
11	BCD Channel No. (1)	Output
12	BCD Channel No. (2)	Output
13	BCD Channel No. (4)	Output
14	BCD Channel No. (8)	Output
15	BCD Channel No. (10)	Output
16	Ground	
17	+12 VDC	Output
18	–12 VDC	Output
19	+170 VDC	Output

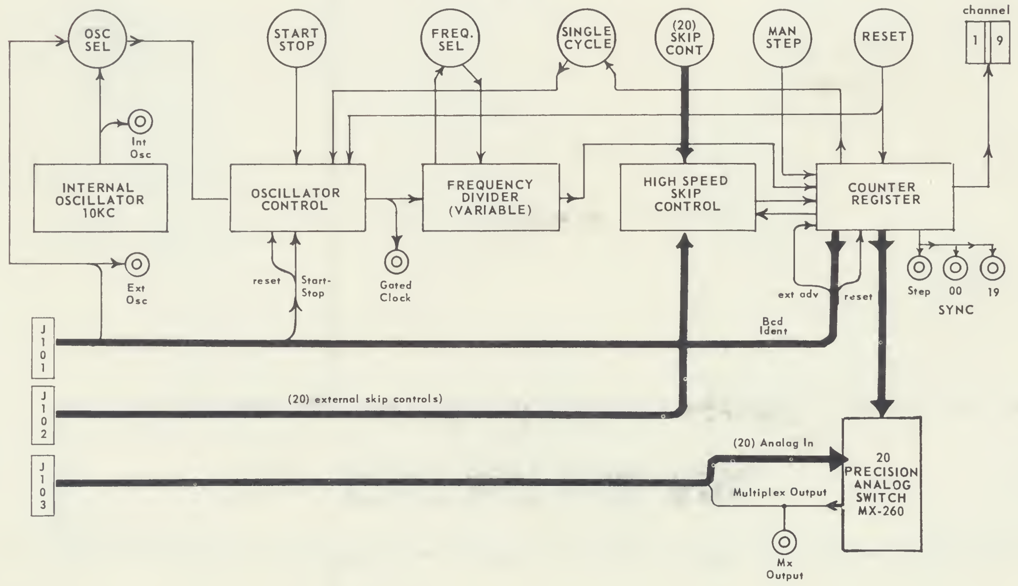
J102
AMPHENOL 57–40500
(Mates With 57–30500)

PIN	FUNCTION	
1	Skip Channel 0	Input
2	Skip Channel 1	Input
3	Skip Channel 2	Input
4	Skip Channel 3	Input
5	Skip Channel 4	Input
6	Skip Channel 5	Input
7	Skip Channel 6	Input
8	Skip Channel 7	Input
9	Skip Channel 8	Input
10	Skip Channel 9	Input
11	Skip Channel 10	Input
12	Skip Channel 11	Input
13	Skip Channel 12	Input
14	Skip Channel 13	Input
15	Skip Channel 14	Input
16	Skip Channel 15	Input
17	Skip Channel 16	Input
18	Skip Channel 17	Input
19	Skip Channel 18	Input
20	Skip Channel 19	Input
21	Ground	
22	Skip Switch Common (0 to 9)	
23	Skip Switch Common (10 to 19)	
24	–12 VDC	Output
25	+12 VDC	Output

J103
AMPHENOL 57–40360
(Mates With 57–30360)

PIN	FUNCTION
1	Data Input Channel 1
2	Data Input Channel 2
3	Data Input Channel 3
4	Data Input Channel 4
5	Data Input Channel 5
6	Data Input Channel 6
7	Data Input Channel 7
8	Data Input Channel 8
9	Data Input Channel 9
10	Data Input Channel 10
11	Data Input Channel 11
12	Data Input Channel 12
13	Data Input Channel 13
14	Data Input Channel 14
15	Data Input Channel 15
16	Data Input Channel 16
17	Data Input Channel 17
18	Data Input Channel 18
19	Data Input Channel 19
20	Data Input Channel 0
21	Multiplex Output
22	Shield Bus
23	+12 VDC Output
24	–12 VDC Output
25	Ground

BLOCK DIAGRAM



DATA SYSTEMS DIVISION

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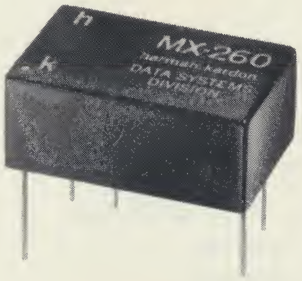
MX-260

MULTIPLEX SWITCH

APPLICATIONS



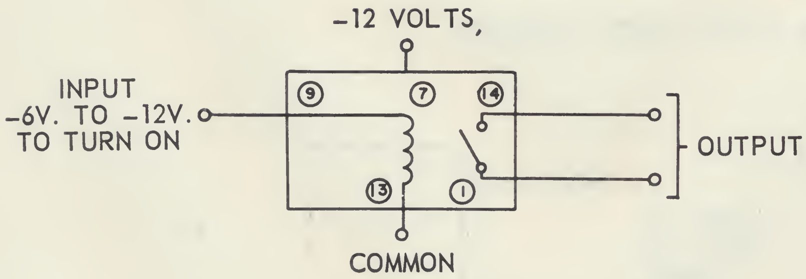
- MULTIPLEXERS
- HIGH SPEED SWITCHING
- VOLTAGE COMPARATOR
- CHOPPERS –
  - STABLE AMPLIFIERS
  - D.C. AMPLIFIERS
- SAMPLE AND HOLD
- REFERENCE VOLTAGE POLARITY REVERSER
- ANALOG COMPUTERS
- DIGITAL METERS
- LOW LEVEL SWITCHING

The Multiplex Switch MX-260 fills the long-standing need for a versatile, high speed, solid state analog switch, combined with reliability, ultra-precision and low cost. A switching speed from D.C. to 10,000 cps is offered, with complete isolation between drive and switching circuits. No drive transformer or external circuitry is required to connect or disconnect a load from the signal source.

The MX-260 module is completely compatible, both electrically and mechanically, with all of the Harman-Kardon standard 200 Series Digital Logic Modules. This offers the necessary flexibility when incorporating the MX-260 into your system requirements.

Eight MX-260 Multiplex Switches can be mounted on one Flexi-Card®, C-1070, for high density packaging; or if desired, arrangement of this module on Flexi-Cards® with other digital logic can be planned so that each Flexi-Card® represents a logical system building block. Both the MX-260 Multiplex Switch and Flexi-Card® C-1070 are available for immediate delivery.

EQUIVALENT CIRCUIT



MX-260 MULTIPLEX SWITCH

MULTIPLEX SWITCH MX-260 SPECIFICATIONS

harman kardon

ELECTRICAL

Input (Signal) Characteristics

Amplitude (Pin 9)	–6v to –12v
Signal (Generator) Impedance	5K max.
Input Impedance	9K nom.
Switching Speed (Square Wave)	DC to 10KC

(The Input Pin 9 may also be shunted to Pin 7, in which case the power supply may be turned on and off to control this unit. The normal power drain will be increased by 0.7ma when the unit is on.)

Output (Contact) Characteristics

Load Impedance	10K min.
Voltage Across Open Contact	±15v max.
Current Through Closed Contact	±1.5ma max.
Contact Resistance (Closed)	36 ohms max.
Offset, Over Full Temperature Range	±100uv max.
Output Noise, Excluding Transients Measured on 200KC Bandwidth	70uv RMS max.
Rise Time + Delay Time	5 usec max.
Storage Time + Fall Time Measured at 1ma	20 usec max.
Leakage (Switch Open) 25°C	.003 ua max.
Leakage (Switch Open) 71°C with 0.5 to 10v Across Contact	.06 ua max.

ISOLATION, SIGNAL TO CONTACT

Resistance	10K megohms min.
Capacity	5 pf max.

POWER SUPPLY

Voltage	–12v ±½v
Current (On Only)	6ma nom.

ENVIRONMENTAL

Temperature, Operating	–30°C to +71°C
Temperature, Storage	–62°C to +85°C
Vibration	±20g's 20 to 2,000 cps
Mounting	Any Position
Life (EMTF)	100,000 hours

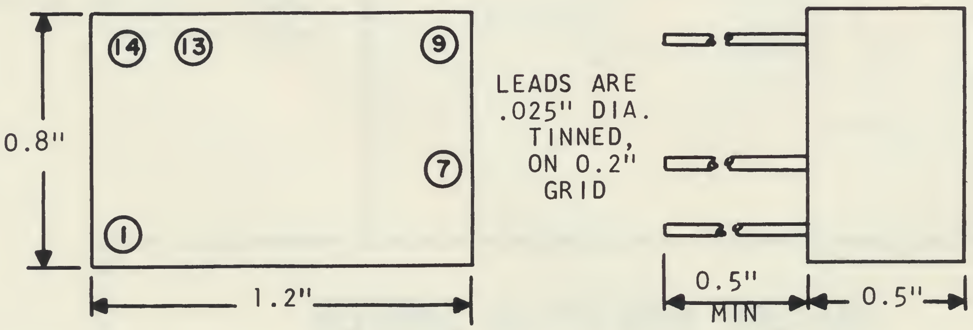
Designed to meet the general requirements of MIL-E-5272C

MECHANICAL

Size	1.2"x 0.8"x 0.5" (0.5 cu. in.)
Color	Green
Weight	0.5 oz.
Outline and Basing	(See Illustration Below)

FULLY COMPATIBLE WITH 100,200 AND 400 SERIES LOGIC LEVELS.

OUTLINE AND BASING



SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

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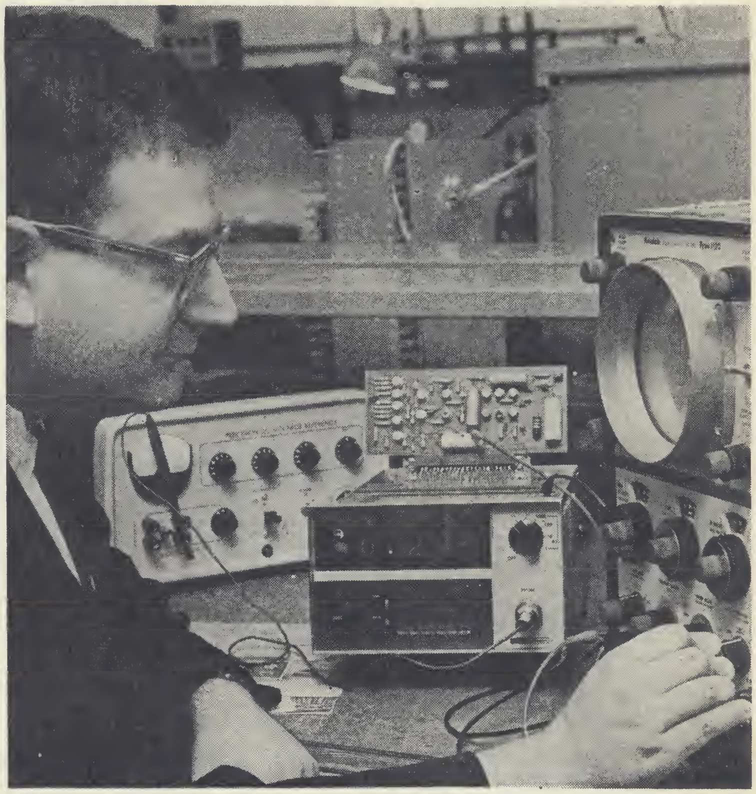


AUTHOR studies the characteristics of his solid-state digital voltmeter

Modified Ramp Generator Develops High D-C Input Impedance

Classical ramp technique is modified for use in a solid-state voltmeter. The result is reduced cost and simplified operation—no input d-c amplifier is needed in most cases

By RICHARD C. WEINBERG
Data Systems Division
Harmon-Kardon, Inc.
Plainview, New York

IN THE DESIGN of a digital voltmeter, if the functions of ramp generator, comparator and flip flop are combined into one circuit designed to have a high d-c input impedance—the result has none of the disadvantages normally associated with digital voltmeters. Mainly, the combination is less expensive and simpler.

Present-day digital voltmeters operate by comparing an internally generated analog voltage with the input voltage. The major difference between the various units is the method of generating the internal comparison voltage. Most units today use a multistep voltage divider operating from a stable standard fixed voltage and controlled by some form of stepping switch. Although the stepping technique is good for accuracies better than 0.01 percent, the stepping switches, precision resistors, and precise voltage standard comprise the major portion of the cost of a fully solid-state unit using this method.

Lesser used techniques are the ramp type and the servo type. Both of these approaches are suitable for accuracies of 0.1 percent. The servo technique involves a motor driven self-balancing potentiometer seeking to null the input against a divided reference. The motor position is mechanically coupled to rotating wheels with painted numbers (like an automobile odometer) for a digital display.

The ramp technique uses an electronically generated linear sweep voltage which moves through uniform, calibrated increments of voltage during each cycle of a precise clock frequency that is usually crystal-controlled. A comparator circuit picks the points in time when the ramp crosses zero volts and crosses the unknown voltage, thereby converting voltage to a time interval which is counted as cycles of the clock.

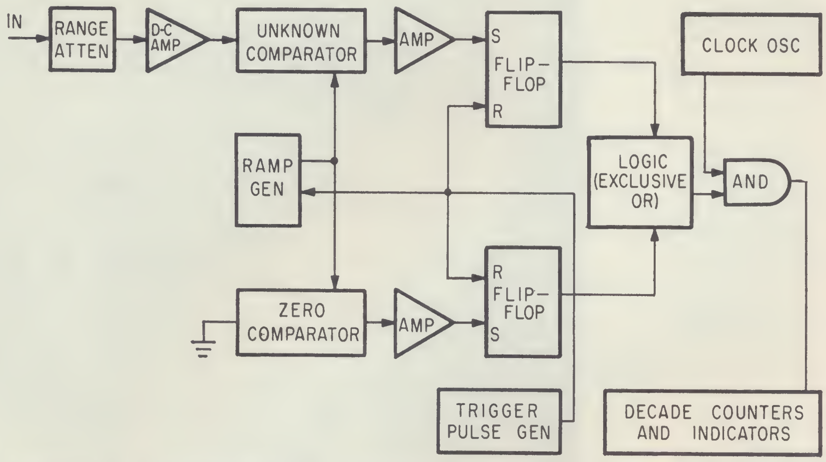
Classical Approach — The ramp-type voltmeter has the configuration shown in Fig. 1. The input signal is processed by an attenuator and amplifier to a uniform full-scale voltage value. The attenuated input is then compared with a precise linear ramp voltage. At the instant of equality, a pulse is generated, setting the UNKNOWN flip flop. Since the starting point and the initial transient on the ramp are not well known, it is difficult to establish a known voltage point on the ramp. Therefore, the zero comparator is

used to produce a pulse as the ramp goes through zero volts (or some other reference voltage). The time between the comparison pulses of the two comparators is proportional to the absolute value of the difference between the unknown voltage and the zero reference voltage. In addition, detecting which of the two flip flops was the first to produce a pulse will give the sign of the unknown voltage compared to the zero reference voltage, since the direction of the ramp slope is known.

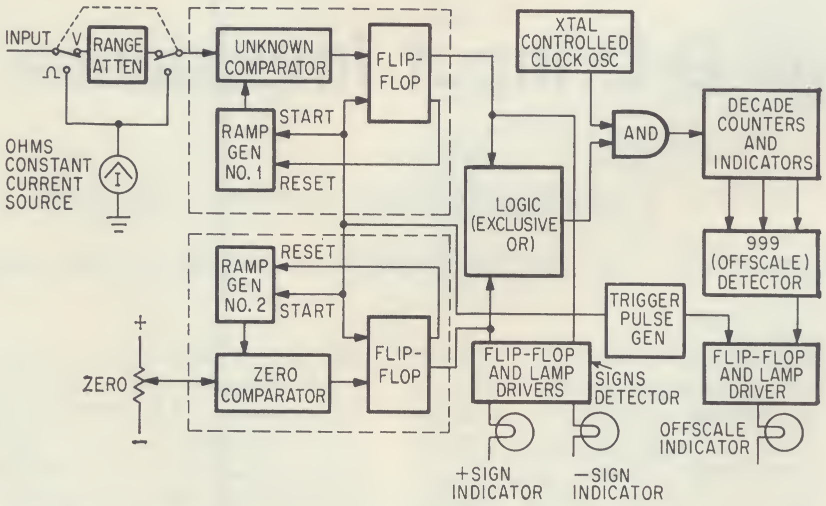
While this system is known to work well, it has several drawbacks. First, commonly used differential comparators cannot drive the logic directly but their outputs must go through amplifying and flip flop stages. Second, (and more important) the comparator itself must present a low impedance to the input signal for a substantial fraction of the time, so that input d-c amplification is essential for isolation.

In the combined approach (figure 2) the ramp generator has to be duplicated. Still, the resultant unit is much simpler, and loads the attenuator with gig-ohm effective impedance levels without an input amplifier. Functions within the dotted lines are accomplished by the new comparator section. An input d-c amplifier is used only in those units required to have a more sensitive scale than the basic 10 volt full scale. Fig. 2 shows the block diagram.

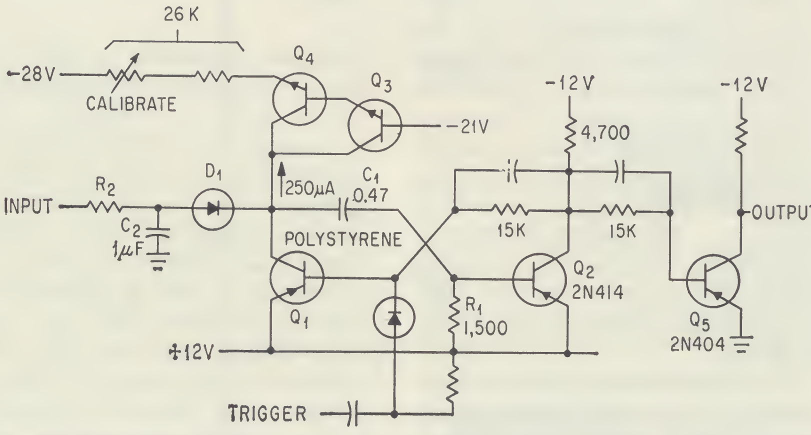
Circuit Details—The circuit chosen for use in the comparator section is shown in Fig. 3. The two pnp transistors, Q_1 and Q_2, are arranged as a monostable multivibrator. In the stable state Q_1 is on and Q_2 is off. When a trigger pulse is received the circuit changes to its quasi-stable state. The constant current regulated by Q_3 and Q_4 is diverted to charge C_1, which charges linearly, producing a ramp of high accuracy. The charging time constant, to a close approximation, is C_1/h_{ob4} (where h_{ob4} is the grounded-base output admittance of Q_4) and can easily be made several thousand times the duration of a comparison cycle. The charging current passing through R_1 produces enough voltage to keep Q_2 turned on. As the ramp voltage passes and begins to exceed the input voltage, some of the charging current is diverted through diode D_1 to charge capacitor C_2. This reduces the voltage across R_1, turning off Q_2, and causing the circuit to return to its stable state. Transistor Q_5 isolates the monostable section from the logic, and restores ground level. The time the circuit is in the quasi-stable state is proportional to the difference between the positive voltage at the emitters of Q_1 and Q_2 and the unknown voltage across C_2. However, drift of the positive voltage (and that of other circuit variables) is cancelled from the reading of the instrument by the use of another, identical cir-



CLASSICAL ramp-type digital voltmeter involves complicated circuits and high cost—Fig. 1



FUNCTIONS of ramp generator, comparator and flip-flop are combined in one circuit (dashed lines) having a high d-c input impedance—Fig. 2



COMPARATOR CIRCUIT uses a silicon alloy chopper (Q_1) to minimize the effects of variation of offset voltage and leakage current—Fig. 3

cuit as the zero-comparator.

The extremely high input impedance of the comparator circuit results from operating D_1 normally cut off. Diode D_1 conducts for only the few microseconds that it takes to reduce the base current of Q_2 sufficiently for regeneration to start. With the total regulated current set at about 250 microamperes, the peak of the current pulse through D_1 is some tens of microamperes, lasting long enough to deliver some 200 picocoulombs into C_2. The average value of the input pulsed current is in the order of 10^{-9} ampere when sampling at its fastest rate of 200 milliseconds. The leakage current of the diode is of this order of magnitude in the opposite direction and ordinarily dominates the input current.

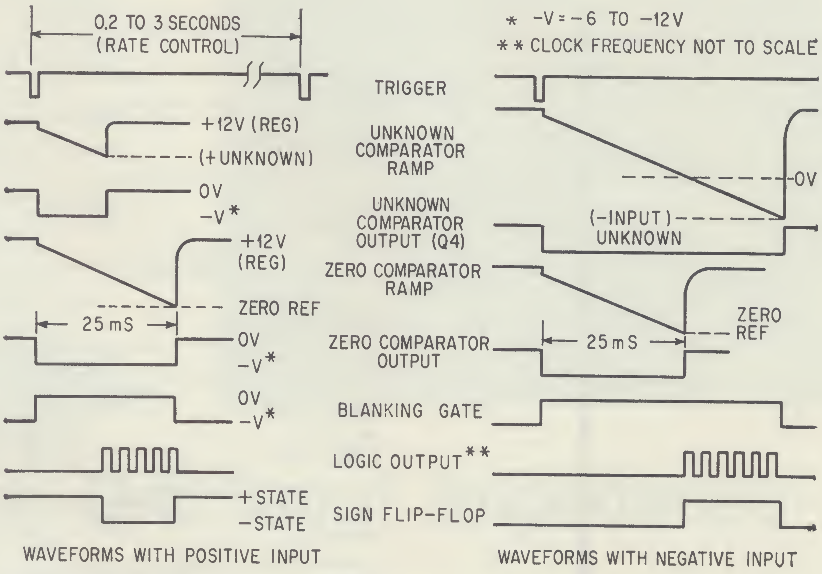
Note that this high impedance is to d-c only. Impedance for a-c input is essentially equal to R_2 because of the necessity of making C_2 a larger value than C_1. The value of C_2 also limits the choice of attenuator source resistance at d-c due to time-constant requirements in charging C_2.

Results—Waveforms produced by the circuit are shown in Fig. 4 and Fig. 6. The ramps start simultaneously but end at different times. When the unknown voltage is positive the input comparator ramp ends before the zero-comparator ramp; when the unknown voltage is negative the input comparator ramp terminates later than the zero comparator ramp. A voltage step equal to the base drop of Q_2 (which is the same as the drop across R_1) precedes the linear portion of the ramp.

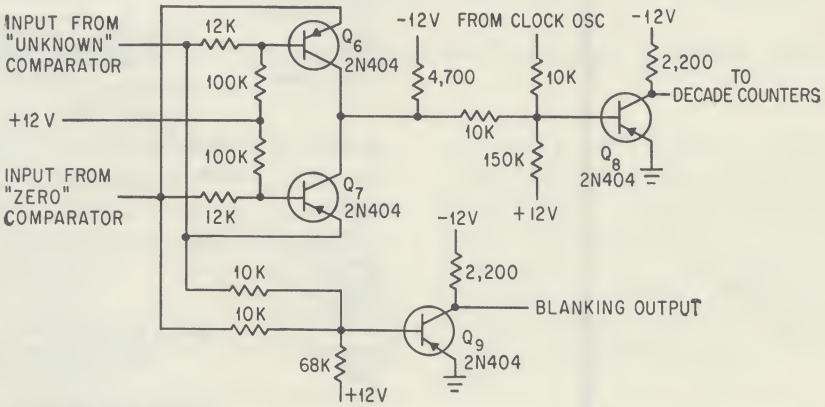
The logic is an exclusive OR gating circuit that produces a ground-level logic signal only when the outputs of the two comparators are in different states. The circuit, which includes transistors Q_6 and Q_7 in Fig. 5, acts as a rectified differential amplifier. A logical ground signal on one input appears also at the output only if the other input is negative enough to saturate the transistor in series with the grounded input. Use of this circuit eliminates the need for complementary inputs required by more conventional types of exclusive logic gates that suffer from the resulting differential delay and pulse leakage. Transistor Q_8 in Fig. 5 gates the clock oscillator (which is continuously running) into the decade counters. Transistor Q_9 generates a blanking gate equal to the duration of the longer comparator ramp. This blanking gate is used to inhibit display and recording of digits and signs during the count-up interval.

A complete measurement, including sign determination, is made following each trigger pulse within 2.5 milliseconds. Measurements may be made at intervals of at least 7 milliseconds to allow circuit recovery. The internal trigger pulse generator is variable from 200 milliseconds to 5 seconds between pulses.

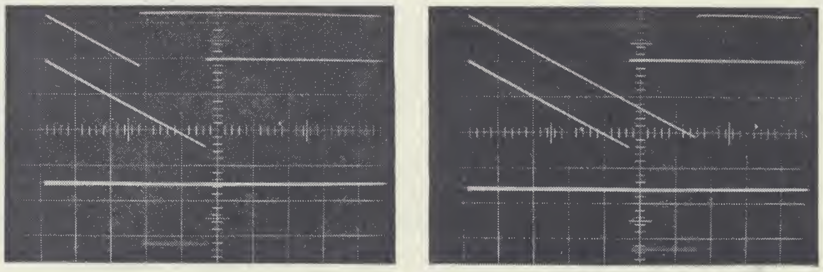
The writer acknowledges the aid of L. J. Torn, Vice President, and R. J. Salzer, Chief Engineer.



WAVEFORMS are produced by the comparator and logic circuits—Fig. 4



LOGIC is an exclusive OR gating circuit that produces a ground level signal only when the output of the two comparators are in different states—Fig. 5



WAVEFORMS result from positive input (left) and negative input (right). The scope traces show: top, the unknown comparator ramp; middle, zero comparator ramp and bottom, the logic output or gated clock pulses. The scales are 5 v per vertical division and 5 ms per horizontal division—Fig. 6

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